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Subject: Software Note: Programming the VME-to-1553 interface board

Introduction

A 'leftover' piece of hardware from Run I is the 6U high VME-to-1553 interface module. This device will be useful during the development of Run II hardware but documentation on how to program the device is absent. This note collects information gleaned from examination of the schematic (copy available in Rick Hance's files), and telephone conversations with the original designers. Obviously, this document cannot encompass the entire MIL-STD-1553 protocol; refer to that specification document for protocol details.

Device Setup

The VMEbus MIL-1553 controller is described by schematic drawing number 0823-ED-28232. Examination of the schematic shows the device to be an A24/D16 VME module which supports interrupts. A DIP switch (SW1) selects the pattern on address lines A[23..16] which are matched to determine the base address of the module. However, the device actually consumes 128K of VME address space, 64K for each of the two independent controllers on the module.

Address Map

Within the 128K address map, the following rules apply. All addresses given are offsets from the device base address as set by the DIP switches.

1. Addresses 0x00000–0x0FFFB map to RAM assigned to 1553 port #1.. However, only 16K of actual RAM is implemented, so in reality only addresses 0x00000–0x03FFB are used.
2. Similarly, addresses 0x10000–0x1FFFB map to RAM assigned to 1553 port #2. Again, only 16K of actual RAM is implemented, so only use addresses 0x10000–0x13FFB.
3. Various 1553 command sequences may be stored in the RAM as desired. To execute a given 1553 command on 1553 port #1, the address within the RAM where the command resides is written to address 0x0FFFC. Performing the write to 0x0FFFC causes the module to immediately process the command. Similarly, a write to address 0x1FFFC causes a 1553 cycle on port #2.
4. The byte at location 0x0FFFE may be read to obtain status of the 1553 data transfer. This requires a D08 transaction. Similarly, for port #2, status is available at 0x1FFFE.
5. If interrupts are desired, the byte at 0x0FFFF (or 0x1FFFF, for port #2), can be written with the interrupt vector desired. Switch SW2 may be used to select IRQs from IRQ1 through IRQ7. The module will then interrupt upon completion of the 1553 sequence. For most operations, interrupts should be disabled by closing all three switches in SW2.
6. The status and interrupt information may be fetched as a 16-bit word by accessing location 0x0FFFE (or, for port #2, 0x1FFFE) using a D16 transfer.

Operation

The generic flow of operation for a 1553 sequence is as follows:

- Determine where in RAM the command is to be stored. The location must be on a word boundary, not a byte boundary.
- Write the value 0x0002 to that location in memory. 0x0002 is an arbitrarily selected value indicating 'start of command'.
- In the next word location in memory, write the 1553 command value which controls the RT address, mode, etc. of the data transfer. Refer to Table 1 below for the bit-wise breakdown.
- If the transaction is a write transaction (transfer of data from VME to the external 1553 device), load the following locations in RAM with the 16-bit data values to be written.
- Write the offset address of the command in RAM, *divided by two*, into address 0x0FFFC (or, for port #2, 0x1FFFC). For example, if the command was stored at RAM location 0x100 (that is, 0x100 above the base address of the module as set by the DIP switches), the value 0x80 (half of 0x100.) must be written to 0x0FFFC.

A more explicit example is useful. Assume the module has been set to address 0x380000 in VME space by setting switch SW1. To write a command to a 1553 device connected to port #1, the value 0x0002 is then written to address 0x380020, within the RAM space for port #1. The 1553 command (RT address, etc.) is written to address 0x380022. Assume the command is a write. The data to write is then stored in locations 0x380024, 0x380026, etc. Once all the data is loaded, to cause the 1553 command to ensue the value 0x0010 (half the offset!) must be written to address 0x38FFFC.

- If the transaction is a read transaction (data flow from external 1553 device to VME interface), the data read will be stored in the RAM in the addresses immediately following the 0x0002 / CMD word pair. The first word will contain the 1553 status information, and successive words will contain the actual data.
- After completion of a write sequence, the 1553 status word will be stored in the RAM location immediately following the last data word written.
- The completion status of the 1553 cycle (separate and distinct from the 1553 status word stored with the data) may be obtained by looking at the byte at address offset 0x0FFE (or, for port #2, 0x1FFE) from the base address. Bit 7 of this byte will be set when the 1553 transaction is complete. If an error occurred, bit 6 will also be set. If bit 6 is set, then execution of the 1553 controller 'get status' command (by writing this into the RAM and running a command sequence) may be used to get detailed error decoding.

Structure of the 1553 Command Value

Whenever a 1553 command sequence is to be performed, the data word immediately following the 0x0002 word must be a Command Value which tells the 1553 interface chip what to do. This sixteen bit value contains five fields as described in Table 1.

Bit (s)	Field Name	Notes
15..11	RT Address	5-bit address of device on 1553 bus. A value of 31 indicates a broadcast to all devices.
10	T/R	If 1, this is a 'transmit', or write, operation. If zero, a 'receive' or read.
9..6	Subaddress/Mode	If 0 or 31, then next five bits are a Mode Code. Otherwise, the internal register number, or Subaddress, to which the data transfer is aimed.
5..1	Word Count/Mode Code	If the Subaddress is 1–30 inclusive, the number of 16-bit words to transfer. In this usage, a value of 0 indicates 32 words. Otherwise, if the Subaddress is 0 or 31, this field is a Mode Code which does not transfer data in/out of the external 1553 device but is instead used to modify the way that external device's 1553 interface functions, in accordance with the MIL-STD-1553 specification.
0	Parity	Odd parity over the preceding 16 bits; that is, parity of the command value.

Table 1

Interpretation of Status Values

Upon completion of the 1553 sequence, a 1553 status word is left in the RAM memory. On writes, the status word is left after the data values; on reads, the status word precedes the data values. This sixteen-bit status value contains numerous bit fields as given in Table 2; for more detailed data, see section 4.3.3.5.3 of the 1553 spec.

Bit(s)	Field Name	Notes
15..11	RT Address	A loopback of the RT address from the external device, which should be the same as what was set in the Command word.
10	Message Error	If set, a transmission error was detected by the external device. This can be a Manchester error or a protocol error.
9	Instrumentation Bit	Should always be zero.
8	Service Request	If set, external device requires service; exactly what is device dependent.
7,6	Reserved status	Should always be zero.
5	Broadcast Received	If set, the 1553 cycle was a Broadcast, or at least that's what the external device believed it was.
4	Busy	If set, command cannot be completed; try again.
3	Subsystem Flag Bit	Optional bit; if set, can indicate fault in external device.
2	Dynamic bus control accepted	If set, external device implements dynamic bus control protocol.
1	Terminal Flag	If set, indicates error specific to use of T/F flag (special mode commands)
0	Parity	Odd parity bit for this word.

Table 2

Other Documentation

A quick search of the Web shows that the Linac group has provided some documentation about how this module was set up for Run I. The following links may provide additional information.

<http://www-linac.fnal.gov/LINAC/software/locsys/syscode/vmesoftware/MilStd1553Handling.html>

<http://www-linac.fnal.gov/LINAC/software/locsys/syscode/vmesoftware/interrupts.html>

<http://www-linac.fnal.gov/LINAC/software/locsys/syscode/vmesoftware/drv1553.html>